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(TITLE OF THE INVENTION)

SEMICONDUCTOR DEVICE, FABRICATION METHOD THEREOF, AND FABRICATION METHOD FOR LEAD FRAME

(CLAIMS)

1. A semiconductor device including a semiconductor chip provided with electrode pads formed to have a first pitch, leads electrically connected to the electrode pads by a wiring, respectively, and a resin encapsulate for encapsulating the semiconductor chip, wherein:

protrusions are formed on the leads, respectively, in such a fashion that they have a second pitch different from the first pitch; and

the resin encapsulate is arranged to encapsulate the wiring connected between the electrode pads and the leads while allowing the protrusions to be exposed.

2. A semiconductor device including a semiconductor chip provided with electrode pads formed to have a first pitch, leads electrically connected to the electrode pads by a wiring, respectively, and a resin encapsulate for encapsulating the semiconductor chip, wherein:

protrusions are formed on the leads, respectively, in

such a fashion that they have a second pitch different from the first pitch; and

the resin encapsulate has a thickness from a surface of the semiconductor chip formed with the electrode pads not more than a height from the semiconductor chip surface to each protrusion, but not less than the height from the semiconductor chip surface to the wiring.

3. The semiconductor device according to claim 1 or 2, wherein the semiconductor chip and the leads are bonded together by an adhesive comprised of a polyimide film.

4. The semiconductor device according to any one of claims 1 to 3, wherein each of the protrusions is formed in such a fashion that it is integrally with an associated one of the leads.

5. The semiconductor device according to any one of claims 1 to 4, wherein the wiring comprises wires.

6. The semiconductor device according to any one of claims 1 to 5, wherein each of the protrusions is formed with a bump.

7. A method for fabricating a semiconductor device

comprising the steps of:

forming leads each provided with a protrusion at a region where an outer connecting terminal is to be formed;

arranging a polyimide film on at least one of the leads and the semiconductor chip, pressing the leads and the semiconductor chip by a desired pressure while interposing the polyimide film between the leads and the semiconductor chip, and heating the polyimide film to a desired temperature to allow the polyimide film to serve as an adhesive, thereby bonding the leads and the semiconductor chip together;

connecting the electrode pads formed on the semiconductor chip to the leads by a wiring, respectively, thereby electrically connecting the electrode pads and the leads together; and

forming a resin encapsulate adapted to partially or completely encapsulating the wiring and the semiconductor chip while allowing each of the protrusions to be exposed at a tip surface thereof.

8. The method according to claim 7, wherein a thermoplastic adhesive is applied to both surfaces of the polyimide film when the leads and the semiconductor chip are bonded together by the polyimide film at the bonding step.

9. The method according to claim 7 or 8, wherein the

electrode pads and the leads are electrically connected together using a direct lead bonding process at the connecting step.

10. A lead frame provided with a plurality of leads each having an inner lead portion and an outer lead portion, wherein the inner lead portion have a lead pitch less than a lead pitch of the outer lead portions, and each of the outer lead portion has a protrusion integrally formed therewith.

11. The lead frame according to claim 10, wherein the lead pitch (Pout) of the outer lead portions is substantially equal to the thickness (W) of each lead at a region where the protrusion is formed, and the lead pitch (Pin) of the inner lead portions corresponds to about half the lead pitch (Pout) of the outer lead portions (Pin = Pout/2).

12. A method for fabricating a lead frame according to claim 10 or 11, comprising:

a primary etching step for conducting a half-etching process for a blank while using a mask arranged on the blank at the protrusion forming region; and

a secondary etching step for conducting a half-etching process for the blank while using a mask arranged on the blank at the lead forming region.

13. A method for fabricating a lead frame according to claim 10 or 11, comprising the steps of:

preparing a first blank and a second blank respectively having thicknesses selected in such a fashion that they have a total thickness corresponding to the height of the protrusions when they are overlapped with each other;

forming a lead pattern having a planar shape corresponding to the shape of the leads on the first blank;

forming a protrusion pattern on the second blank in such a fashion that the protrusion pattern is arranged at the protrusion forming region;

overlapping the first blank formed with the lead pattern and the second blank formed with the protrusion pattern together, and bonding the first and second blanks to each other in such a fashion that the lead pattern and the protrusion pattern are overlapped with each other at the protrusion forming region; and

removing unnecessary portions of the first and second blanks.

14. A method for fabricating a lead frame according to claim 10 or 11 comprising the steps of:

forming a lead pattern having a planar shape corresponding to a shape of the leads on a blank; and

forming the protrusions at a desired region on the lead

pattern after completion of the lead pattern forming step.

15. The method according to claim 14, wherein the protrusion forming step is achieved by overlapping one or more bumps on the lead pattern at a desired region to form the protrusion.

16. The method according to claim 14, wherein the protrusion forming step is achieved by arranging a conductive member on the lead pattern at a desired region to form the protrusion.

17. The method according to claim 14, wherein the protrusion forming step is achieved by subjecting a desired portion of the lead pattern to a plastic shaping process to form the protrusion.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a semiconductor device, a method for fabricating the semiconductor device, and a method for fabricating a lead frame used in the semiconductor device. In particular, the present invention relates to a semiconductor device having a structure encapsulating a semiconductor chip and leads by resin, a method for fabricating the semiconductor

device, and a method for fabricating a lead frame used in the semiconductor device.

The recent trend of electronic appliances to be downsized has resulted in efforts to achieve an increased density and increased mounting efficiency of semiconductor devices. It is also expected to obtain an improvement in the reliability of electronic appliances. In addition, there is demand for an improvement in the reliability of semiconductor devices. Furthermore, it is expected for semiconductor devices to achieve a reduction in costs.

Accordingly, developments of semiconductor devices capable of satisfying the above mentioned demands are strongly required.

[DESCRIPTION OF THE PRIOR ART]

Recently, a flip chip type mounting structure has been proposed as a scheme capable of achieving a high-density mounting. Such a flip chip type mounting structure is widely used in multi chip modules (MCMs). In accordance with the flip chip mounting scheme applied to MCMs, no resin encapsulate is formed. Instead, bumps are formed on electrode pads of a semiconductor chip (bare chip), respectively. In this case, mounting of the bare chip is achieved by bonding the bare chip to electrode portions formed on a circuit board (mother board) in a face down bonding fashion.

In accordance with the use of the flip chip type mounting structure, it is possible to mount semiconductor devices on a mother board at a high density. An improvement in electrical characteristics is also achieved because the semiconductor devices are electrically connected to the mother board by means of bumps directly formed on the bare chips of the semiconductor devices.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

However, the bare chips not encapsulated by resin involve problems in that they exhibit a degradation in heat resistance, mechanical strength, and temperature resistance. Furthermore, since bumps are directly formed on electrode pads formed on each bare chip, the layout of the electrode pads formed on the bare chip is rendered to be the layout of outer connecting terminals (bumps) as it is.

Generally, semiconductor chips have different layouts of electrode pads thereof in accordance with the manufacturers thereof. Accordingly, even for semiconductor devices having the same function, the user should design a wiring pattern of the mother board to match the kind of those semiconductor devices (manufacturer). In the conventional mounting structure using bare chips, there are problems of a degradation in the matching ability of semiconductor devices to the mother board and an increased burden to the user because no standardization for

outer electrode terminals of semiconductor devices is made.

In order to solve the above mentioned problems, the standardization may probably be made by processing the surface of a chip and forming a wiring on the processed chip surface. However, this scheme requires a number of processes with a high accuracy to form a desired wiring. Furthermore, there are problems of an increase in costs and a degradation in the efficiency of production.

The present invention has been made in view of the above mentioned problems, and an object of the invention is to provide a semiconductor device, a method for fabricating the semiconductor device, and a method for fabricating a lead frame used in the semiconductor device, which are capable of achieving a standardization of outer electrode terminals to keep the reliability of a semiconductor chip used, a reduction in costs, and an improvement in the efficiency of production.

(MEANS FOR SOLVING THE SUBJECT MATTERS)

The above subject matters can be solved by the following means.

The invention of claim 1 is characterized by a semiconductor device including a semiconductor chip provided with electrode pads formed to have a first pitch, leads electrically connected to the electrode pads by a wiring, respectively, and a resin encapsulate for encapsulating the

semiconductor chip, wherein: protrusions are formed on the leads, respectively, in such a fashion that they have a second pitch different from the first pitch; and the resin encapsulate is arranged to encapsulate the wiring connected between the electrode pads and the leads while allowing the protrusions to be exposed.

The invention of claim 2 is characterized by a semiconductor device including a semiconductor chip provided with electrode pads formed to have a first pitch, leads electrically connected to the electrode pads by a wiring, respectively, and a resin encapsulate for encapsulating the semiconductor chip, wherein: protrusions are formed on the leads, respectively, in such a fashion that they have a second pitch different from the first pitch; and the resin encapsulate has a thickness from a surface of the semiconductor chip formed with the electrode pads not more than a height from the semiconductor chip surface to each protrusion, but not less than the height from the semiconductor chip surface to the wiring.

The invention of claim 3 is characterized by the semiconductor device according to claim 1 or 2, wherein the semiconductor chip and the leads are bonded together by an adhesive comprised of a polyimide film.

The invention of claim 4 is characterized by the semiconductor device according to any one of claims 1 to 3, wherein each of the protrusions is formed in such a fashion that

it is integrally with an associated one of the leads. The invention of claim 5 is characterized by the semiconductor device according to any one of claims 1 to 4, wherein the wiring comprises wires.

The invention of claim 6 is characterized by the semiconductor device according to any one of claims 1 to 5, wherein each of the protrusions is formed with a bump. The invention of claim 4 is characterized by a method for fabricating a semiconductor device comprising the steps of: forming leads each provided with a protrusion at a region where an outer connecting terminal is to be formed; arranging a polyimide film on at least one of the leads and the semiconductor chip, pressing the leads and the semiconductor chip by a desired pressure while interposing the polyimide film between the leads and the semiconductor chip, and heating the polyimide film to a desired temperature to allow the polyimide film to serve as an adhesive, thereby bonding the leads and the semiconductor chip together; connecting the electrode pads formed on the semiconductor chip to the leads by a wiring, respectively, thereby electrically connecting the electrode pads and the leads together; and forming a resin encapsulate adapted to partially or completely encapsulating the wiring and the semiconductor chip while allowing each of the protrusions to be exposed at a tip surface thereof.

The invention of claim 8 is characterized by the method

according to claim 7, wherein a thermoplastic adhesive is applied to both surfaces of the polyimide film when the leads and the semiconductor chip are bonded together by the polyimide film at the bonding step.

The invention of claim 9 is characterized by the method according to claim 7 or 8, wherein the electrode pads and the leads are electrically connected together using a direct lead bonding process at the connecting step.

The invention of claim 10 is characterized by a lead frame provided with a plurality of leads each having an inner lead portion and an outer lead portion, wherein the inner lead portion have a lead pitch less than a lead pitch of the outer lead portions, and each of the outer lead portion has a protrusion integrally formed therewith.

The invention of claim 11 is characterized by the lead frame according to claim 10, wherein the lead pitch (Pout) of the outer lead portions is substantially equal to the thickness (W) of each lead at a region where the protrusion is formed, and the lead pitch (Pin) of the inner lead portions corresponds to about half the lead pitch (Pout) of the outer lead portions (Pin = Pout/2). The invention of claim 12 is characterized by a method for fabricating a lead frame according to claim 10 or 11, comprising: a primary etching step for conducting a half-etching process for a blank while using a mask arranged on the blank at the protrusion forming region; and a secondary etching step for

conducting a half-etching process for the blank while using a mask arranged on the blank at the lead forming region.

The invention of claim 13 is characterized by a method for fabricating a lead frame according to claim 10 or 11, comprising the steps of: preparing a first blank and a second blank respectively having thicknesses selected in such a fashion that they have a total thickness corresponding to the height of the protrusions when they are overlapped with each other; forming a lead pattern having a planar shape corresponding to the shape of the leads on the first blank; forming a protrusion pattern on the second blank in such a fashion that the protrusion pattern is arranged at the protrusion forming region; overlapping the first blank formed with the lead pattern and the second blank formed with the protrusion pattern together, and bonding the first and second blanks to each other in such a fashion that the lead pattern and the protrusion pattern are overlapped with each other at the protrusion forming region; and removing unnecessary portions of the first and second blanks.

The invention of claim 14 is characterized by a method for fabricating a lead frame according to claim 10 or 11 comprising the steps of: forming a lead pattern having a planar shape corresponding to a shape of the leads on a blank; and forming the protrusions at a desired region on the lead pattern after completion of the lead pattern forming step.

The invention of claim 15 is characterized by the method

according to claim 14, wherein the protrusion forming step is achieved by overlapping one or more bumps on the lead pattern at a desired region to form the protrusion.

The invention of claim 16 is characterized by the method according to claim 14, wherein the protrusion forming step is achieved by arranging a conductive member on the lead pattern at a desired region to form the protrusion.

The invention of claim 17 is characterized by the method according to claim 14, wherein the protrusion forming step is achieved by subjecting a desired portion of the lead pattern to a plastic shaping process to form the protrusion.

[FUNCTIONS]

Each of the above mentioned means serves as follows.

In accordance with the invention of claims 1 and 2, it is possible to achieve an improvement in heat resistance, mechanical strength, and temperature resistance. Since the electrode pads and leads are connected together using wires, it is possible to set the layout of the leads irrespective of the layout of the electrode pads. An improvement in the matching ability of the semiconductor device to the circuit board. The resin encapsulate provides an improvement in reliability because it surely protects the connected wires. Since the outer connecting terminals are exposed from the resin encapsulate, the electrical connection of the semiconductor device to the circuit

board can be surely provided.

In accordance with the invention of claim 3, the insulating and bonding processes for the semiconductor chip and leads can be simultaneously conducted because the polyimide film, as an insulating member, interposed between the semiconductor chip and the leads serves as an adhesive. Accordingly, it is possible to simplify the structure of the semiconductor device while achieving an easy fabrication of the semiconductor device, as compared to the case in which the insulating member and the adhesive are separately provided.

In accordance with the invention of claim 4, each protrusion is integrally formed with an associated one of the leads. Accordingly, it is possible to achieve a simplification in structure, as compared to the case in which the protrusion and lead are formed using separate materials, respectively. In accordance with the invention of claim 5, a wire is used for the connection between the electrode pad and lead. Accordingly, it is possible to achieve an easy connection for the wire between the electrode pad and lead.

In accordance with the invention of claim 6, a bump is formed on each protrusion. Accordingly, it is possible to achieve an easy connection of the semiconductor device to the circuit board, as compared to the case in which the protrusion is directly mounted on the circuit board. In accordance with the invention of claim 7, the leads and semiconductor chip are

bonded together by maintaining the polyimide film at a certain temperature and a certain pressure, thereby causing the polyimide film to serve as an adhesive. Accordingly, the insulating and bonding processes for the leads and semiconductor chip can be simultaneously conducted.

Since each electrode pad formed on the semiconductor chip is connected to an associated one of the leads by means of a wire in the bonding process, it is possible to vary the layout of the leads with respect to the layout of the electrode pads by selecting an appropriate connection method. The fabrication of the semiconductor device involves only four processes, that is, a lead forming process, a bonding process, a connecting process, and a resin encapsulating process. Since the fabrication of semiconductor device is achieved using a reduced number of processes, as mentioned above, an improvement in production efficiency is obtained.

In accordance with the invention of claim 8, an easy bonding process can be achieved because the bonding process can be conducted without a control for the temperature applied to the polyimide film within a desired range.

In accordance with the invention of claim 9, the connection between the electrode pads and the leads can be simply and surely achieved because the electrode pads and leads are electrically connected together in accordance with a direct lead bonding process. In accordance with the invention of claim

10 and 11, the lead pitch of the outer lead portions is less than the lead pitch of the inner lead portions. Accordingly, the inner leads can cope with a small pitch of the electrode pads on the semiconductor chip to which the inner lead portions are electrically connected. Furthermore, the mounting efficiency of the semiconductor device to the circuit board is improved because the lead pitch of the outer lead portions electrically connected to the circuit board is large. Since each protrusion is formed on an associated one of the outer lead portions, it can be used as an outer connecting terminal. Accordingly, it further improves the mounting efficiency.

In accordance with the invention of claim 12, it is possible to form leads each integrally formed with a protrusion by conducting a primary etching process for the blank in accordance with a half-etching method in such a fashion that the blank has a reduced thickness at its portion except for the region to be formed with the protrusions and then conducting a secondary etching process for the thickness-reduced portion of the blank to form the leads.

The pitch of the leads is determined by the thickness of the blank upon forming the leads. In other words, it is only possible to form leads having a pitch substantially equal to the thickness of the blank. Accordingly, a reduced lead pitch can be obtained when the blank has a reduced thickness.

Meanwhile, where leads provided with protrusions are

formed, the thickness of the blank is determined by the height of the protrusions. It is impossible to form leads having a small pitch by simply etching the blank having a thickness equal to the height of the protrusions. In accordance with the present invention, however, it is possible to form leads having a small pitch, even when the leads have a structure provided with protrusions, by conducting a primary etching process for the blank in accordance with a half-etching method in such a fashion that the blank has a reduced thickness at its portion except for the region to be formed with the protrusions, and then conducting a secondary etching process for the thickness-reduced portion of the blank to form the leads. As apparent from the above description, the pitch of the protrusions can be reduced to a pitch substantially equal to the thickness of the blank.

In accordance with the invention of claim 13, the first and second blanks have thicknesses respectively selected in such a fashion that they have a total thickness corresponding to the height of the protrusions when they are overlapped with each other. For this reason, each of the first and second blanks has a thickness less than the height of the protrusions. In the lead pattern forming step, a lead pattern having the same shape as the whole shape of the leads is formed on the thin first blank. Accordingly, it is possible to reduce the lead pitch of the lead pattern formed in accordance with the above mentioned

relation between the blank thickness and lead pitch.

In the protrusion pattern forming step, a protrusion pattern is formed on the second blank in such a fashion that it is arranged at the protrusion forming region. In the bonding step, the first and second blanks are bonded together in a state in which they are overlapped with each other. The lead pattern and protrusion pattern are overlapped with each other at the protrusion forming region. The blank thickness at the protrusion forming region corresponds to a desired height of the protrusions. At the removing step, unnecessary portions of the blanks are removed, thereby forming leads.

Accordingly, a reduction in lead pitch is achieved because the thickness of the blank used in the formation of the lead pattern is small. On the other hand, since the lead pattern and protrusion pattern are overlapped with each other at the protrusion forming region, it is possible to form protrusions having a desired thickness. In accordance with the invention of claim 14, the lead pattern forming step and the protrusion forming step are conducted in a separate fashion. Accordingly, the thickness of a blank used can be selected irrespective of the height of the protrusion. Therefore, it is possible to reduce the pitch of a lead pattern when a thin blank is used. In the protrusion forming process, it is possible to form protrusions having an optional height. An improvement in the freedom of design is also achieved.

In accordance with the invention of claims 15 to 17, it is possible to easily conduct the protrusion forming process.

[EMBODIMENTS]

Now, preferred embodiments of the present invention will be described in conjunction with the annexed drawings. Figs. 1 and 2 illustrate a semiconductor device 1 according to an embodiment of the present invention. Fig. 1 is a cross-sectional view of the semiconductor device 1 whereas Fig. 2 is a bottom view of the semiconductor device 1.

As shown in the figures, the semiconductor device 1 mainly includes a semiconductor chip 2, a plurality of leads 3, a resin encapsulate 4, and bumps 5. The semiconductor chip 2 is provided at the central portion of its lower surface with a plurality of electrode pads 6 arranged in a line. Each of the leads 3 has an inner lead portion 3a and an outer lead portion 3b. The leads 3 are bonded to the lower surface of the semiconductor chip 2 by means of a polyimide film 7.

The polyimide film 7 serves as an insulating member for electrically insulating the leads 3 from a circuit surface 2A formed on the lower surface of the semiconductor chip 2. The polyimide film 7 also serves as an adhesive for bonding the leads 3 to the semiconductor chip 2 as described hereinafter. Since the polyimide film 7 functions as both the insulating member and the adhesive, it is possible to simplify the

structure of the semiconductor cevice 1 which achieving an easy fabrication of the semiconductor device 1, as compared to the case in which the insulating member and the adhesive are separately provided.

Wires 8 are arranged between the inner leads 3a and the electrode pads 6 of the semiconductor chip 2, respectively. The semiconductor chip 2 is electrically connected with the leads 3 by the wires 8, respectively. A protrusion 9 is formed at a desired position of the outer lead portion 3b included in each lead 3 in such a fashion that it is integral with the outer lead portion 3b. In most cases, the leads 3 having the above mentioned structure are arranged on the lower surface of the semiconductor chip 2. This arrangement is called a "lead on chip (LOC)" structure. By virtue of this arrangement, the semiconductor device 1 can be miniaturized.

The resin encapsulate 4 is made of, for example, epoxy resin. This resin encapsulate 4 is formed in accordance with a molding process, as described hereinafter. The resin encapsulate 4 is disposed at the lower surface and side surfaces of the semiconductor chip 2 to have desired thicknesses, respectively. In the illustrated embodiment, the resin encapsulate 4 does not exist at the upper surface of the semiconductor chip 2, that is, a heat dissipation surface.

The resin encapsulate 4 is configured in such a fashion that its thickness (indicated by the arrows H) from the surface

of the semiconductor chip 2 formed with the electrode pads 6, that is, the lower surface of the resin encapsulate 4, is not more than the height (indicated by the arrows W) from the lower surface of the resin encapsulate 4 to the tip of the protrusion 9, but not less than the height (indicated by the arrows h) from the lower surface of the resin encapsulate 4 to the apex of a roof of the wire 8 ($h \leq H \leq W$). By virtue of this configuration, at least the tip 9a of each protrusion 9 is surely exposed from the resin encapsulate 4. In this case, the wires 8 and the leads 3, except for the exposed portions of the protrusions 9, are encapsulated by the resin encapsulate 4.

Since the semiconductor device 1 of this embodiment is configured in such a fashion that a desired portion of the semiconductor chip (that is, the portion except for the upper surface) is encapsulated by the resin encapsulate, it is possible to achieve an improvement in heat resistance, mechanical strength, and temperature resistance. Also, an improvement in the reliability of the semiconductor device 1 is achieved because the resin encapsulate 4 surely protects the wires 8. In addition, it is possible to surely obtain an electrical connection to a circuit board 10 because at least the tip 9a of each protrusion 9 serving as an outer connection terminal is surely exposed from the resin encapsulate 4.

Now, a description will be made in conjunction with a plurality of leads 3 arranged on the lower surface of the

semiconductor chip 2 while referring to Fig. 2. For the convenience of description, the resin encapsulate 4 arranged on the lower surface of the semiconductor chip 2 is removed from Fig. 2. As shown in Fig. 2, the leads 3 are configured in such a fashion that the lead pitch of adjacent inner lead portions 3a (indicated by the arrows Pin) is less than the lead pitch of adjacent outer lead portions 3b (indicated by the arrows Pout). In detail, the lead pitch Pin of the inner lead portions 3a corresponds to about half the lead pitch Pout of the outer lead portions 3b (Pin = Pout/2). The lead pitch Pout of the outer lead portions 3b is substantially equal to the thickness W of each lead 3 at a region where the protrusion 9 is formed.

Since the lead pitch Pin of the inner lead portions 3a is small as compared to the lead pitch Pout of the outer lead portions 3b, the inner lead portions 3a can cope with a possible small pitch of the electrode pads 6 of the semiconductor chip 2 to which the inner lead portions 3a are electrically connected. On the other hand, since the lead pitch Pout of the outer lead portions 3b (protrusions 9) electrically connected to the circuit board 10 is large, it is possible to achieve an improvement in the mounting efficiency of the semiconductor device 1 on the circuit board 10.

Meanwhile, the semiconductor device 1 according to the illustrated embodiment has a configuration in which the electrical connection of the electrode pads 6 arranged on the

semiconductor chip 2 to the circuit board 10 is not achieved by the bumps 5 directly formed on the electrode pads 6, but achieved by the wires 8 arranged between the electrode pads 6 and the inner leads 3a. Accordingly, an electrical signal from each electrode pad 6 can be transferred to the outside of the semiconductor device 1 via the associated lead 3 and wire 8. This makes it possible to set the layout of the leads 3 irrespective of the layout of the electrode pads 6.

In the case of Fig. 2, electrical signals from the electrode pads 6 centrally formed on the semiconductor chip 2 are outwardly transferred via the wires 8 and leads 3. Also, the protrusions 9, which serve as outer connecting terminals, are arranged at the peripheral portion of the semiconductor chip 2. Where the electrode pads 6 are formed at the peripheral portion of the semiconductor chip 2, as shown in Fig. 3, it is possible to arrange the protrusions 9 serving as outer connecting terminals at a region inside the electrode pads 6 because electrical signals from the electrode pads 6 can be outwardly transferred via the wires 8 and leads 3. Furthermore, the protrusions 9 serving as outer connecting terminals may be arranged at a region outside the semiconductor chip 2, as shown in Fig. 4.

Since electrical signals from the electrode pads 6 can be outwardly transferred using the leads and wires 8, an improvement in the matching ability of the semiconductor device

1 to the circuit board 10 is achieved. It is also possible to easily set the layout of the protrusions 9, which serve as outer connecting terminals, to be the layout of standard outer connecting terminals. Accordingly, a reduction in the burden to the user of the semiconductor device 1 is achieved.

Now, a method for fabricating the semiconductor device 1 having the above mentioned configuration will be described. The semiconductor device 1 according to the present invention is fabricated using four basic processes, that is, a lead forming process, a bonding process, a connecting process, and a resin encapsulating process, along with two additional processes, that is, a bump forming process and a testing process. The fabrication method will be described in conjunction with the above mentioned processes, respectively.

Figs. 5 to 9 illustrate a first embodiment associated with the lead forming process. This lead forming process is a process for forming a lead frame 11 which is a blank for forming the leads 3. For the formation of the lead frame 11, a flat blank 12 is first prepared, as shown in Fig. 5. The blank 12 may be a lead frame blank made of, for example, 42 ALLOY and having a thickness corresponding to the height W of the protrusions 9.

Thereafter, a mask 13 (indicated by small dots) is arranged on the blank 12, as shown in Fig. 6. The mask 13 covers a region (denoted by the reference numeral 14) to be

formed with the protrusions 9 and a region (denoted by the reference numeral 15) to be formed with cradles.

After the arrangement of the mask 13, a half-etching process (primary etching process) is conducted for the blank 12. In the illustrated embodiment, the half-etching process for the blank 12 is carried out in accordance with a wet etching method (of course, other etching methods, for example, a dry etching method, may be used). The etching time is set so that the thickness of an etched portion (the white portion in Fig. 6) corresponds to about half the thickness W of the blank 12 (W/2).

Fig. 7 shows a state in which the mask 13 is removed after completion of the half-etching process. In this state, the blank 12 maintains the thickness W only at its portion corresponding to the region 14 to be formed with protrusions 9 and its portion corresponding to the region 15 to be formed with cradles 15. The remaining portion of the blank 12 (denoted by the reference numeral 16) has a thickness corresponding to W/2 by virtue of the half-etching.

After completion of the half-etching process as mentioned above, the blank 12 is subjected to another etching process under the condition in which a mask 17 (indicated by small dots) is arranged to cover a region (denoted by the reference numeral 18) to be formed with leads 3 along with the region 15 to be formed with cradles.

In accordance with the etching process (secondary etching

process), the portions of the blank 12 not covered with the mask 17 are removed. Thus, a lead frame 11 provided with a plurality of leads 3 having a structure as shown in Fig. 9 is obtained. If necessary, silver may be plated on a desired portion of the lead frame 11 (corresponding to the region formed with the leads 3).

The lead frame 11 formed as mentioned above has a structure in which each lead 3 has an inner lead portion 3a, an outer lead portion 3b, and a protrusion 9 integrally formed together. In this structure, the protrusion 9 has a thickness corresponding to W whereas the inner lead portion 3a and the outer lead portion 3b except for its part corresponding to the region formed with the protrusion 9 have a thickness corresponding to W/2.

The relation between the lead pitch and the thickness of the blank 12 will now be described. The pitch of the leads 3 is determined by the thickness of the blank 12 upon forming the leads 3. In other words, it is only possible to form leads having a pitch substantially equal to the thickness of the blank 12. Accordingly, a reduced lead pitch can be obtained when the blank 12 has a reduced thickness.

Meanwhile, where leads 3 provided with protrusions 9 are formed, the thickness of the blank 12 is determined by the height of the protrusions 9. It is impossible to form leads having a small pitch by simply etching the blank 12 having a

thickness equal to the height of the protrusions 9. In accordance with the present invention, however, it is possible to form leads 3 having a small pitch (the lead pitch Pin in Fig. 11a), even when the leads 3 have a structure provided with protrusions 9, by conducting a primary etching process for the blank 12 in accordance with a half-etching method in such a fashion that the blank 12 has a reduced thickness (a thickness corresponding to about W/2) at its portion except for the region 14 to be formed with the protrusions 9, and then conducting a secondary etching process for the thickness-reduced portion of the blank 12 to form the leads 3. For the same reason, the pitch Pout of the protrusions 9 (outer lead portions 3b) can be reduced to a pitch substantially equal to the thickness W of the blank 12.

For instance, where a typical lead frame blank having a thickness of 0.10 mm is used, it is possible to obtain a minimum pitch Pout of the outer lead portions 3b and protrusions 9 corresponding to 0.10 mm (Pout = 0.10 mm) and a minimum pitch Pin of the inner lead portions 3a corresponding to 0.05 mm (Pin = 0.05 mm). In the case of a typical lead frame blank having a thickness of 0.15 mm, it is possible to obtain a minimum pitch Pout of the outer lead portions 3b and protrusions 9 corresponding to 0.15 mm (Pout = 0.15 mm) and a minimum pitch Pin of the inner lead portions 3a corresponding to 0.075 mm (Pin = 0.075 mm). Where a typical lead frame blank having a thickness

of 0.20 mm is used, it is possible to obtain a minimum pitch Pout of the outer lead portions 3b and protrusions 9 corresponding to 0.20 mm (Pout = 0.20 mm) and a minimum pitch Pin of the inner lead portions 3a corresponding to 0.11 mm (Pin = 0.10 mm).

On the other hand, the position of each protrusion 9 is determined by the position of the mask 13 shown in Fig. 6. That is, the position of each protrusion 9 can be optionally determined by appropriately varying the position of the mask 13. For this reason, the positions of the protrusions 9 serving as outer connecting terminals can be set within a certain degree of freedom in accordance with a lead forming method included in the illustrated embodiment. Therefore, it is possible to easily form the protrusions 9 at predetermined positions for standard outer connecting terminals, respectively.

Next, a second embodiment associated with the lead forming process will be described. Figs. 10 to 15 illustrate the second embodiment associated with the lead forming process. For the formation of a lead frame 20 in this embodiment, a first blank 21 shown in Fig. 10 and a second blank 22 shown in Fig. 11 are first prepared.

The thicknesses of the blanks 21 and 22 are determined so that the total thickness obtained in an overlapping state of the blanks 21 and 22 corresponds to the height W of each protrusion 9. In this embodiment, the thicknesses of the blanks 21 and 22

are set to be W/2, respectively. The blanks 21 and 22 have different thicknesses, respectively, in so far as the total thickness obtained in an overlapping state of the blanks 21 and 22 corresponds to the height W of each protrusion 9.

The first blank 21 shown in Fig. 10 is made of a lead frame material such as 42 ALLOY. This first blank 21 has a structure formed with a lead pattern 23 having the same pattern shape as that of the leads 3 when viewed in a plan view. This structure of the first blank 21 is obtained by previously conducting an etching process or a press-punching process for the first blank 21. However, the lead pattern 23 of the first blank 21 has no protrusion in accordance with this lead forming process, as different from the lead forming process in which the protrusions 9 are formed. Accordingly, the lead pattern 23 has a thickness of W/2 at the entire portion thereof. In Fig. 10, the reference numeral 25 denotes a position determining slot which is formed during the formation of the lead pattern 23.

On the other hand, the second blank 22 shown in Fig. 11 is made of a lead frame material such as 42 ALLOY. This second blank 22 has a structure formed with a protrusion pattern 24. This structure of the second blank 22 is obtained by conducting an etching process or a press-punching process for the second blank 22. The protrusion pattern 24 has a straight line pattern shape. In the protrusion pattern 24, regions to be formed with a certain number of protrusions 9 are arranged in parallel while

being laterally spaced from one another. In Fig. 11, the reference numeral 26 denotes a position determining slot which is formed during the formation of the protrusion pattern 24.

The first and second blanks 21 and 22 having the above mentioned structures are then overlapped with each other by vertically aligning the position determining slots 25 and 26 with each other. In the overlapping state, the first and second blanks 21 and 22 are bonded together. The bonding of the first and second blanks 21 and 22 may be achieved using a conductive adhesive or a welding process. Fig. 12 shows the bonded state of the first and second blanks 21 and 22.

In the bonded state of the first and second blanks 21 and 22, the protrusion pattern 24 of the second blank 22 overlaps with protrusion forming regions on the lead pattern 23 of the first blank 22.

Fig. 13 is a plan view illustrating, in a enlarged scale, the overlapping region between the lead pattern 23 and protrusion pattern 24. Also, Fig. 14 is a cross-sectional view illustrating, in an enlarged scale, the overlapping region between the lead pattern 23 and protrusion pattern 24. As shown in Figs. 13 and 14, the lead pattern 23 having a thickness of W/2 corresponding to half the total thickness of the blanks overlaps, in a cross fashion, with the protrusion pattern 24 having a thickness of W/2 corresponding to half the total thickness of the blanks. Accordingly, the regions to be formed

with the protrusions 9 have a thickness W corresponding to the total blank thickness. Accordingly, this thickness W is rendered to be the height of each protrusion 9 (Fig. 14).

After completion of the bonding process for the first and second blanks 21 and 22, the resulting structure is partially removed at its portion except for the portion where the lead pattern 23 and protrusion pattern 24 cross, using a pressing process or the like, thereby forming a lead frame 20 having leads 3 integrally formed with protrusions 9, as shown in Fig. 15.

Similarly to the lead frame 11 fabricated in accordance with the first embodiment, each lead 3 of the lead frame 20 fabricated in accordance with this embodiment has an inner lead portion 3a, an outer lead portion 3b, and a protrusion 9 integrally formed together. In accordance with this embodiment, the lead pattern 23 can be formed to have a small pitch because the first blank 21 has a thickness corresponding to W/2. This will be apparent by referring to the above mentioned relation between the lead pitch and the blank thickness.

Meanwhile, the position of each protrusion 9 is determined by the position of the protrusion pattern 24 formed at the second blank 22. That is, the position of each protrusion 9 can be optionally determined by appropriately varying the position of the protrusion pattern 24. For this reason, the positions of the protrusions 9 serving as outer

connecting terminals can be set within a certain degree of freedom in accordance with the lead forming method included in this embodiment. Therefore, it is possible to easily form the protrusions 9 at predetermined positions for standard outer connecting terminals, respectively.

After the lead frame 11 or 20 (in the following description, only the lead frame 11 will be referred) is fabricated in accordance with the above mentioned lead forming process, a bonding process for bonding the lead frame 11 and semiconductor chip 2 together is conducted. Now, the bonding process will be described in conjunction with Figs. 16 to 20.

In this bonding process, gold is plated on the inner lead portions 3a of the lead frame 11 at regions where wires 8 are to be bonded in a subsequent connecting process, thereby forming bonding areas 27, as shown in Fig. 16.

Also, a polyimide film 7 is arranged on the surface of the semiconductor chip 2 formed with the electrode pads 6 in such a fashion that only the electrode pads 6 are exposed. The polyimide film 7 is made of a polyimide material having a glass transition point of 100 to 300 °C. In the state of Fig. 17, the polyimide film 7 is simply in a state laid on the semiconductor chip 2. In order to prevent the polyimide film 7 from being separated from the semiconductor chip 2, accordingly, the semiconductor chip 2 is arranged in such a fashion that its surface formed with the electrode pads 6 is upwardly positioned.

In other words, the semiconductor chip 2 is in a bare chip state not encapsulated by resin. The polyimide film 7 may be previously formed on the semiconductor chip 2 during a wafer process for forming the semiconductor chip 2.

Subsequently, the lead frame 11 shown in Fig. 18 is laid on the semiconductor chip 2 on which the polyimide film 7 is laid. The leads 3 (inner lead portions 3a) formed on the lead frame 11 face, in a high accuracy, the electrode pads 6 formed on the semiconductor chip 2. Thus, the position of the lead frame 11 is determined.

After the lead frame 11 is laid in position on the semiconductor chip 2, as mentioned above, a die 28 is lowered to press the lead frame 11 against the semiconductor chip 2, as shown in Fig. 19. The die 28 is equipped with a heating unit. Heat generated from the die 28 is applied to the polyimide film 7 via the lead frame 11.

The polyimide film 7 typically serves as an insulating member for electrically insulating the semiconductor chip 2 and lead frame 11 from each other, as in conventional cases. However, the inventors found the fact that the polyimide film 7 can serve as an adhesive when it is under a certain condition. In detail, where the polyimide film 7 is made of a polyimide material having a glass transition point of 100 to 300°C, it can serve as an adhesive when it is heated to a temperature higher than the glass transition point by 100 to 200°C while being

applied with a pressure of 1 to 10 Kgf/cm².

In view of the above mentioned fact, the polyimide film is heated to a temperature higher than the glass transition point by 100 to 200°C by the heater equipped in the die 28 upon bonding the semiconductor chip 2 and lead frame 11 to each other while being applied with a pressure of 1 to 10 Kgf/cm² by the die 28 in accordance with the present invention. Accordingly, the polyimide film 7 can serve as an adhesive. Thus, it is possible to bond the semiconductor chip 2 and lead frame 11 to each other by means of the polyimide film 7.

In accordance with the above mentioned configuration, it is unnecessary to use a separate adhesive for bonding the semiconductor chip 2 and lead frame 11 to each other, as compared to conventional cases using a polyimide film. Accordingly, it is possible to achieve a reduction in costs and a reduction in the number of processing steps used in the fabrication of the semiconductor device 1. Fig. 20 illustrates a state in which the semiconductor chip 2 and lead frame 11 are bonded to each other by the polyimide film 7.

Although the bonding between the semiconductor chip 2 and lead frame 11 is achieved in accordance with the bonding method using the polyimide film 7, it may be achieved using other methods. For example, the bonding between the semiconductor chip 2 and lead frame 11 may be achieved using a method in which an adhesive is applied to both surfaces of the polyimide film

interposed between the semiconductor chip 2 and lead frame 11, as in conventional cases. Where this method is used, it is unnecessary to carry out a temperature control and a pressure control for the polyimide film. Accordingly, the bonding process is simply achieved.

After the semiconductor chip 2 and lead frame 11 are bonded to each other in accordance with the bonding process, a connecting process is carried out to electrically connect the leads 3 formed on the lead frame 11 to the electrode pads 6 formed on the semiconductor chip 2 by means of wires 8, respectively.

Fig. 21 illustrates a process for mounting each wire (for example, a gold wire) 8 between the bonding pad 27 (Fig. 16) formed on an associated one of the leads 3 and an associated one of the electrode pads 6 using capillaries 29. As well known, it is desirable for each wire 8 to be short in terms of an improvement in the electrical characteristics of the semiconductor device 1. On the other hand, in terms of a miniaturization and thinness of the semiconductor device 1, it is desirable for each wire 8 to have a low roof.

For this reason, it is preferred that a low-roof bonding process be used in mounting the wires 8. For such a low-roof bonding process, a variety of methods are known. For example, a method may be used in which each wire 8 is bonded at one end thereof to an associated one of the electrode pad 6 formed on

the semiconductor chip 2 and then bonded at the other end thereof to an associated one of the leads 3 by upwardly moving the capillary 29 associated with the other end of the wire 8, and then horizontally moving the capillary 29. A method called a "reverse stamping method" may also be used.

Since the leads 3 and electrode pads 6 are electrically connected together in accordance with the wire bonding process, it is possible to achieve the connecting process in an easy fashion and in a high accuracy. The shaping and connection of each wire 8 between the associated lead 3 and electrode pad 6 can be carried out within a certain degree of freedom. Fig. 22 illustrates the state of each wire 8 mounted between the associated lead 3 and electrode pad 6 after the connecting process is conducted.

After the leads and electrode pads 6 are electrically connected together in accordance with the connecting process, a resin encapsulating process is carried out to form a resin encapsulate 4 at a desired portion of the semiconductor chip 2. This resin encapsulating process will now be described in conjunction with Figs. 23 to 25.

Fig. 23 illustrates a state in which the semiconductor chip 2 mounted with the lead frame 11 and wires 8 is loaded in a mold 30. The mold 30 includes an upper mold 31 and a lower mold 32. The lead frame 11 is clamped between the upper and lower molds 31 and 32. Thus, the semiconductor chip 2 is mounted in

the mold 30.

The upper mold 31 is configured to come into contact with the protrusions 9 and the cradles 33 of the lead frame 11 in a loaded state of the semiconductor chip 2. Since the protrusions 9 have the same height as the cradles 33, the upper mold 31 maintains a flat plate shape. The lower mold 32 has a cavity defined with a space at each side of the semiconductor chip 2 loaded in the lower mold 32. The lower surface of the semiconductor chip 2 is in contact with the lower surface of the cavity 33.

Since the upper mold 31 used in the resin encapsulating process has a flat plate shape, and the cavity 33 defined in the lower mold 32 has a simple structure, it is possible to reduce the costs taken in the manufacture of the mold 30. Accordingly, a reduction in the costs taken in the fabrication of the semiconductor device 1 can be achieved.

Fig. 24 illustrates a state in which a resin encapsulate 4 (indicated by a number of small dots) is molded in the mold 30. As the resin encapsulate 4 is molded in the mold 30, the peripheral surface of the semiconductor chip 2 except for its upper surface (viewed as a lower surface in Figs. 23 to 25) contacting the lower mold 32 is encapsulated by the resin encapsulate 4. The leads 3 and wires 8 mounted to the lower surface of the semiconductor chip 2 are also encapsulated by the resin encapsulate 4. Also, each protrusion 9 except for its

portion contacting the upper mold 31 is encapsulated by the resin encapsulate 4.

Fig. 25 illustrates a state in which the semiconductor chip 2 encapsulated by the resin encapsulate 4 is unloaded from the mold 30. As shown in this figure, the upper surface 2a of the semiconductor chip 2 is exposed from the resin encapsulate 4. Accordingly, it is possible to effectively dissipate heat generated from the semiconductor chip 2 at the exposed upper surface 2a. The end 9a of each protrusion 9 is also outwardly exposed from the resin encapsulate 4. Accordingly, the end 9a can be used as an outer connecting terminal.

A semiconductor device is obtained by cutting the lead frame 11 from the structure shown in Fig. 25 along portions indicated by a dotted line in Fig. 25. Although this semiconductor device can achieve the same effect as the semiconductor device shown in Fig. 1, it exhibits a degradation in the mounting efficiency thereof to the circuit board 10 because the end 9a of each protrusion 9 serving as an outer connecting terminal is substantially flush with the surface of the resin encapsulate 4, as shown in Fig. 25. To this end, in accordance with the illustrated embodiment, a bump forming process for forming a bump 5 on the end 9a is conducted after completion of the resin encapsulating process. Hereinafter, the bump forming process will be described in conjunction with Figs. 26 to 30.

In the bump forming process, the semiconductor chip 2 encapsulated by the resin encapsulate 4 is subjected to a honing process at the entire surface thereof, as shown in Fig. 26. By this honing process, a resin layer existing on the end 9a of each protrusion 9 is completely removed, there causing the end 9a to be completely exposed. After completion of the honing process, the semiconductor chip 2 encapsulated by the resin encapsulate 4 is immersed in a solder bath 34, thereby causing the end 9a of each protrusion 9 to be plated by solder. The plated solder film is denoted by the reference numeral 35. The solder used in the solder plating process may be one having a composition of Pb : Sn = 1 : 9. Fig. 28 shows a state in which a solder film 35 is formed on the end 9a of each protrusion 9 in accordance with the solder plating process.

After completion of the above mentioned solder plating process, a bump 5 is formed on the end 9a of each protrusion 9 formed with the solder film 35. The formation of the bump 5 may be carried out using various methods. For example, a conventional bump forming method capable of effectively and easily forming bumps 5 may be used. Fig. 29 shows a state in which bumps 5 are formed on the ends 9a of the protrusions 9, respectively.

After the formation of the bump 5 on the end 9a of each protrusion 9, a process for cutting the lead frame 11 at positions indicated dotted lines in Fig. 29 is carried out.

After the cutting process is completed, a semiconductor device 1 shown in Fig. 30 is obtained. Prior to the process for cutting the lead frame 11, the portions of the lead frame 11 to be cut may be subjected to a half-etching process in order to allow the cutting process to be more easily conducted.

A testing process is then conducted for the semiconductor device 1 fabricated as mentioned above, in order to determine whether or not the fabricated semiconductor device 1 operates normally. Figs. 31 to 33 illustrate different testing methods for the semiconductor device 1, respectively. The testing method shown in fig. 31 uses a socket 36 having a configuration for mounting the bumps 5. In accordance with this testing method, a test such as a burning test is conducted in a state the semiconductor device 1 is mounted on the socket 36.

The testing method shown in Fig. 32 is a method for testing the semiconductor device 1 using probes 37. The semiconductor device 1 has a structure in which the end of each lead 3 is exposed from the side surface of the resin encapsulate 4. In view of this structure of the semiconductor device 1, the testing method is adapted to test the semiconductor device 1 using the probes 37 contacting the leads 3 exposed from the resin encapsulate 4. In accordance with this testing method, it is possible to conduct the testing process even after the semiconductor device 1 is mounted on the circuit board 10.

Fig. 33 illustrates a mounting process for mounting the

semiconductor device 1 on the circuit board 10. The process for mounting the semiconductor device 1 on the circuit board 10 can be achieved using a variety of well-known methods. For instance, an infrared reflow method may be used. In accordance with this infrared reflow method, each bump 5 formed on the semiconductor device 1 is temporarily fixed to an associated one of electrode portions 38 formed on the circuit board 10 suing a paste. The bump 5 is then melted by an infrared reflow furnace arranged over the semiconductor device 1, thereby causing it to be bonded to the associated electrode portion 38.

Now, examples modified from the above mentioned semiconductor device fabrication method will be described. Figs. 34 to 37 illustrate modified structures of the protrusions 9, respectively. Figs. 34A and 34B illustrate a protrusion 9A having a circular column shape, respectively. Also, Fig. 34C illustrates a protrusion 9B having a square column shape. That is, the protrusion may have various planar shape, as in the protrusions 9, 9A, and 9B. The protrusion can have an optional shape in accordance with the bonding characteristics of the bump 5 and the shape of the electrode portion 38 formed on the circuit board 10. For example, the protrusion 9, 9A or 9B is formed using an etching method, it can have a desired planar shape by appropriately selecting the shape of the mask 13 arranged at the protrusion forming region 14 shown in Fig. 6.

The protrusion may also have a structure provided with a

round recess at the upper surface thereof, as in the protrusion 9C shown in Fig. 35(A). Also, the protrusion may have a structure provided with a lump at a central portion of the upper surface thereof, as in the protrusion 9D shown in Fig. 35B. The protrusion may also have a structure provided with a rectangular recess at a central portion of the upper surface thereof, as in the protrusion 9E shown in Fig. 35C. In all the protrusions 9C to 9E, it is possible to obtain an increased protrusion surface area resulting in an improvement in the bondability to the bump 8. Furthermore, the protrusions 9C to 9E are adapted to be fixed to the lead 3 at a desired protrusion forming region.

Referring to Fig. 35D, a protrusion 9F is illustrated which is formed in accordance with a direct plastic deformation of the lead 3 by a pressing process. In this case, the protrusion 9F can be easily formed using a desired process such as a pressing process. However, this method has a problem in that the protrusion 9F cannot have a height more than a limitation for the plastic deformation.

Referring to Fig. 36, a protrusion 9G is illustrated which is formed by forming a stud bump at a desired protrusion forming region in accordance with a wire bonding technique. Fig. 36A illustrates a method for forming the protrusion 9G whereas Fig. 36B illustrates, in an enlarged scale, the protrusion 9G.

Where the protrusion 9G is formed to have a stud bump

shape in accordance with a wire bonding technique, it is possible for the protrusion 9G to be formed at an optional position. The protrusion 9G serving as an outer connecting terminal can also be easily formed at a desired position. The formation of the protrusion 9G can be achieved simultaneously with the mounting of the wires 9 conducted in the connecting process included in the semiconductor device fabrication process. Thus, the entire fabrication process is simplified.

The height of the protrusion 9G can be optionally set by vertically overlapping a plurality of stud bumps together. Referring to Fig. 37A, a protrusion 9H is illustrated which is formed by vertically overlapping three stud bumps together. In this case, the protrusion 9H has an increased height, as compared to the protrusion 9G of Fig. 36B constituted by one stud bump.

Another method for increasing the height of the protrusion is illustrated in Fig. 37B. In accordance with the method of Fig. 37B, a conductive member 41 having a plug shape is fixed to the lead 3 by means of a conductive adhesive. A stud bump 42 is then formed on the conductive member 41, as shown in Fig. 37C, so that the overlapping conductive member 41 and stud bump 42 cooperate to form a protrusion 9I. In this case, the height of the protrusion 9I is determined by the height of the conductive member 41. Accordingly, the height of the protrusion 9I can be optionally set by using a plug-shaped

conductive member having a diverse size for the plug-shaped conductive member 41.

Fig. 38 illustrates a modified bonding process. Although the semiconductor chip 2 and lead frame 11 are bonded together using the polyimide film 7 serving as an adhesive under a certain condition in accordance with the above mentioned embodiment, as shown in Figs. 16 to 20, they may be bonded together using a tape-shaped adhesive 45 in place of the polyimide film 7.

The tape-shaped adhesive 45 may be formed not only at the upper surface of the semiconductor chip 2, but also at the lower surface of the lead frame 11, as shown in Fig. 39. Alternatively, the tape-shaped adhesive 45 may be formed only at the lower surface of the lead frame. Furthermore, the distribution range of the tape-shaped adhesive 45 may be freely set in so far as it is within a range indicated by the arrow X in Fig. 38, except for the region where the electrode pads 6 are formed. In addition, it is necessary for the tape-shaped adhesive 45 to be an insulating adhesive because the semiconductor chip 2 and lead frame 11 should be electrically insulated from each other.

Figs. 39 to 42 illustrate modified embodiments of the connecting process, respectively. Although the wires 8 are used for the connection between the electrode pads 6 and the leads 3 in accordance with the above mentioned embodiment, as shown in

Figs. 21 and 22, a direct lead bonding method is used to directly bond the electrode pads and leads 3 together in accordance with the modified embodiments of Figs. 39 to 42.

In the embodiment of Figs. 39 and 40, each lead 3 is directly bonded to an associated one of the electrode pads 6 using a bonding tool 46 connected to, for example, an ultrasonic vibrator. In this configuration, however, the electrode pad 6 may be damaged by the bonding tool 46 vibrating at an ultrasonic frequency. In the embodiment of Figs. 41 and 42, a stud bump 47 is mounted on each electrode pad 6. The stud bump 47 is then melted by a heating unit 48 in a state in which it comes into contact with the lead 3, thereby causing the electrode pad 6 to be connected to the lead 3. In accordance with this connecting method, there is no damage to the electrode pad 6. An improvement in the reliability of the connecting process is also achieved.

In accordance with the connecting processes of Figs. 39 to 42, it is possible to achieve a reduction in electrical resistance, as compared to a configuration in which the connection between the electrode pads 6 and the leads 3 is provided by the wires 8. Accordingly, an improvement in the electrical characteristics of the semiconductor device 1 is achieved. The semiconductor device 1 also cope with a high-speed semiconductor chip.

Figs. 43 and 44 illustrated a modified embodiment of the

resin encapsulating process. In the above mentioned embodiment, the bottom surface of the cavity defined in the lower mold 31 included in the mold 30 is in direct contact with the upper surface 2a of the semiconductor chip 2. The upper surface 2a of the semiconductor chip 2 is not encapsulated by the resin encapsulate 4 so that it serves as a surface for improving the heat dissipation characteristics.

Under strict environment, for example, high-temperature environment, the semiconductor device 1 may require a temperature resistance rather than the heat dissipation characteristics. In such a case, it is necessary to completely encapsulate the semiconductor chip 2 by the resin encapsulate 4. Referring to Figs. 43 and 44, a mold 50 is illustrated which is configured to completely encapsulate the semiconductor chip 2 by the resin encapsulate 4.

In detail, a cavity 52 defined in a lower mold 51 is spaced apart from the peripheral surface of the semiconductor chip 2 at its side surface, as shown in Fig. 43. Accordingly, when the resin encapsulate 4 is molded in the mold, the semiconductor chip 2 is completely encapsulated by the resin encapsulate 4, as shown in Fig. 44. The formation region of the resin encapsulate 4 encapsulating the semiconductor chip 2 can be optionally set by appropriately varying the shape of the cavity 33 or 52 of the mold 30 or 50.

Where the upper mold 31 has a recess for mounting the

protrusion 9 formed on each lead 3 therein, it is possible to obtain a semiconductor device 60 in which the protrusion 9 is greatly protruded from the resin encapsulate 4, as shown in Fig. 45. The semiconductor device 60 shown in Fig. 45 exhibits an improved mounting efficiency to the circuit board 10 because the protrusion 9 is greatly protruded from the resin encapsulate 4. Also, it is unnecessary to form the bumps 5, as in the above mentioned embodiments. Accordingly, it is possible to simplify the fabrication process for the semiconductor device 60.

[EFFECTS OF THE INVENTION]

As apparent from the above description, various effects are obtained in accordance with the present invention.

In accordance with the invention of claims 1 and 2, it is possible to achieve an improvement in heat resistance, mechanical strength, and temperature resistance. Since the electrode pads and leads are connected together using wires, it is possible to set the layout of the leads irrespective of the layout of the electrode pads. An improvement in the matching ability of the semiconductor device to the circuit board. The resin encapsulate provides an improvement in reliability because it surely protects the connected wires. Since the outer connecting terminals are exposed from the resin encapsulate, the electrical connection of the semiconductor device to the circuit board can be surely provided.

In accordance with the invention of claim 3, the insulating and bonding processes for the semiconductor chip and leads can be simultaneously conducted because the polyimide film, as an insulating member, interposed between the semiconductor chip and the leads serves as an adhesive. Accordingly, it is possible to simplify the structure of the semiconductor device which achieving an easy fabrication of the semiconductor device, as compared to the case in which the insulating member and the adhesive are separately provided.

In accordance with the invention of claim 4, each protrusion is integrally formed with an associated one of the leads. Accordingly, it is possible to achieve a simplification in structure, as compared to the case in which the protrusion and lead are formed using separate materials, respectively. In accordance with the invention of claim 5, a wire is used for the connection between the electrode pad and lead. Accordingly, it is possible to achieve an easy connection for the wire between the electrode pad and lead.

In accordance with the invention of claim 6, a bump is formed on each protrusion. Accordingly, it is possible to achieve an easy connection of the semiconductor device to the circuit board, as compared to the case in which the protrusion is directly mounted on the circuit board. In accordance with the invention of claim 7, the leads and semiconductor chip are bonded together by maintaining the polyimide film at a certain

temperature and a certain pressure, thereby causing the polyimide film to serve as an adhesive. Accordingly, the insulating and bonding processes for the leads and semiconductor chip can be simultaneously conducted.

Since each electrode pad formed on the semiconductor chip is connected to an associated one of the leads by means of a wire in the bonding process, it is possible to vary the layout of the leads with respect to the layout of the electrode pads by selecting an appropriate connection method. The fabrication of the semiconductor device involves only four processes, that is, a lead forming process, a bonding process, a connecting process, and a resin encapsulating process. Since the fabrication of semiconductor device is achieved using a reduced number of processes, as mentioned above, an improvement in production efficiency is obtained.

In accordance with the invention of claim 8, an easy bonding process can be achieved because the bonding process can be conducted without a control for the temperature applied to the polyimide film within a desired range. In accordance with the invention of claim 9, the connection between the electrode pads and the leads can be simply and surely achieved because the electrode pads and leads are electrically connected together in accordance with a direct lead bonding process.

In accordance with the invention of claim 10 and 11, the lead pitch of the outer lead portions is less than the lead

pitch of the inner lead portions. Accordingly, the inner leads can cope with a small pitch of the electrode pads on the semiconductor chip to which the inner lead portions are electrically connected. Furthermore, the mounting efficiency of the semiconductor device to the circuit board is improved because the lead pitch of the outer lead portions electrically connected to the circuit board is large. Since each protrusion is formed on an associated one of the outer lead portions, it can be used as an outer connecting terminal. Accordingly, it further improves the mounting efficiency.

In accordance with the invention of claim 12 and 13, it is possible to easily form leads of a small pitch integrally formed with protrusions. In accordance with the invention of claim 14, the lead pattern forming process and the protrusion forming process are conducted in a separate fashion. Accordingly, the thickness of a blank used can be selected irrespective of the height of the protrusion. Therefore, it is possible to reduce the pitch of a lead pattern when a thin blank is used. In the protrusion forming process, it is possible to form protrusions having an optional height. An improvement in the freedom of design is also achieved.

In accordance with the invention of claims 15 to 17, it is possible to easily conduct the protrusion forming process.